

# CBTD3306

## Dual bus switch with level shifting

Rev. 10 — 19 March 2021

Product data sheet

## 1. General description

The CBTD3306 dual FET bus switch features independent line switches. Each switch is disabled when the associated output enable ( $\overline{nOE}$ ) input is HIGH.

The CBTD3306 is characterized for operation from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ .

## 2. Features and benefits

- Designed to be used in 5 V to 3.3 V level shifting applications with internal diode
- $5\ \Omega$  switch connection between two ports
- TTL-compatible input levels
- Multiple package options
- $I_{\text{OFF}}$  circuitry provides partial Power-down mode operation
- Latch-up protection exceeds 100 mA per JESD78B
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - CDM JESD22-C101E exceeds 1000 V

## 3. Ordering information

Table 1. Ordering information

Type number	Package		Version
	Name	Description	
CBTD3306PW	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 4.4 mm	SOT530-1
CBTD3306GT	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body $1 \times 1.95 \times 0.5$ mm	SOT833-1

## 4. Marking

Table 2. Marking codes

Type number	Marking code
CBTD3306PW	D306
CBTD3306GT	W06

## 5. Functional diagram

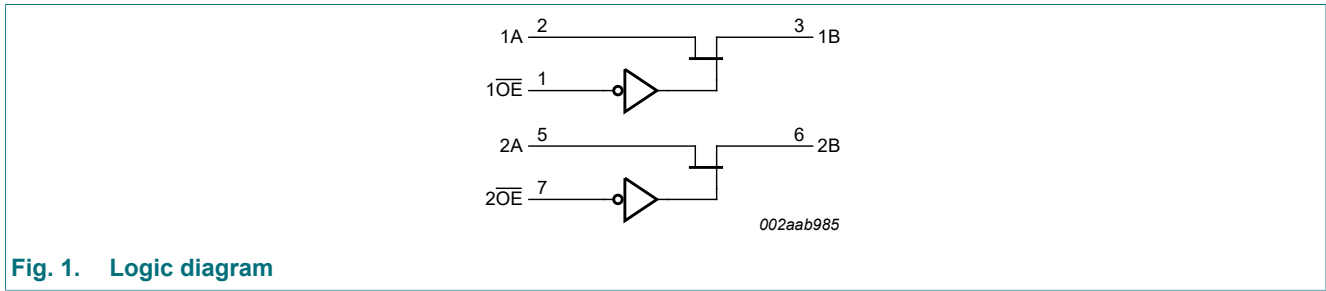


Fig. 1. Logic diagram

## 6. Pinning information

### 6.1. Pinning

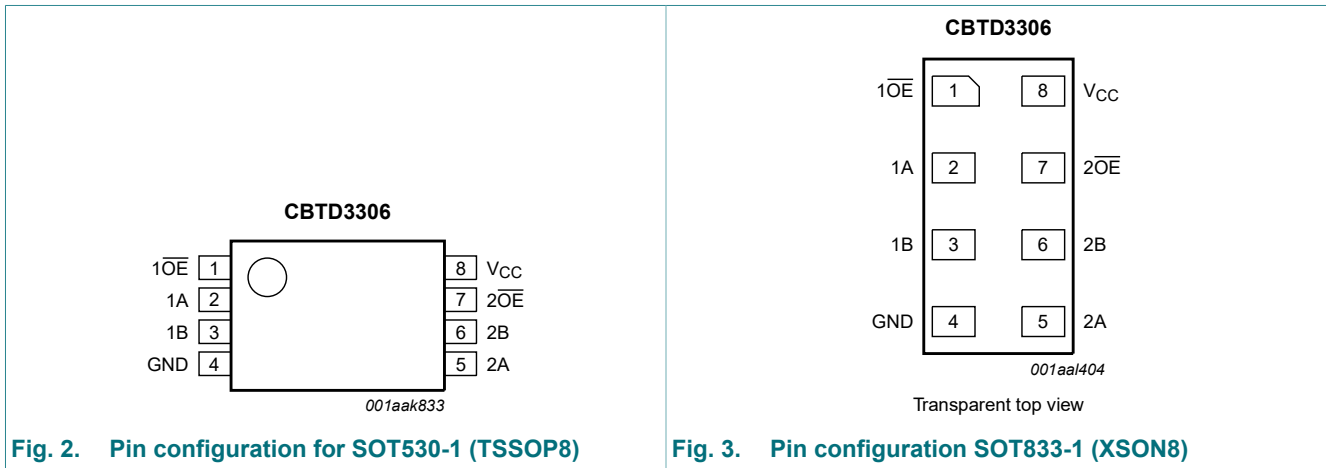


Fig. 2. Pin configuration for SOT530-1 (TSSOP8)

Fig. 3. Pin configuration SOT833-1 (XSON8)

### 6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
1OE, 2OE	1, 7	output enable input
1A, 2A	2, 5	data input/output (A port)
1B, 2B	3, 6	data input/output (B port)
GND	4	ground (0 V)
VCC	8	positive supply voltage

## 7. Functional description

Table 4. Function selection

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

Input	Input/output
nOE	nA, nB
L	nA = nB
H	Z

## 8. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

$T_{amb} = -40\text{ °C to }+85\text{ °C}$ , unless otherwise specified.

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$V_I$	input voltage	[1]	-0.5	+7.0	V
$I_{SW}$	switch current		-	128	mA
$I_{IK}$	input clamping current	$V_{IO} = 0\text{ V}$	-50	-	mA
$T_{stg}$	storage temperature		-65	+150	°C

[1] The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

## 9. Recommended operating conditions

**Table 6. Operating conditions**

All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		4.5	-	5.5	V
$V_{IH}$	HIGH-level input voltage		2.0	-	-	V
$V_{IL}$	LOW-level input voltage		-	-	0.8	V
$T_{amb}$	ambient temperature	operating in free air	-40	-	+85	°C

## 10. Static characteristics

**Table 7. Static characteristics**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	$T_{amb} = -40\text{ °C to }+85\text{ °C}$			Unit
			Min	Typ [1]	Max	
$V_{IK}$	input clamping voltage	$V_{CC} = 4.5\text{ V}; I_I = -18\text{ mA}$	-	-	-1.2	V
$I_I$	input leakage current	$V_{CC} = 5.5\text{ V}; V_I = \text{GND or } 5.5\text{ V}$	-	-	$\pm 1$	$\mu\text{A}$
$I_{CC}$	supply current	$V_{CC} = 5.5\text{ V}; I_{SW} = 0\text{ mA}; V_I = V_{CC}\text{ or GND}$	-	-	1.5	mA
$V_{pass}$	pass voltage	see Fig. 4 to Fig. 8	-	-	-	V
$\Delta I_{CC}$	additional supply current	per input pin; $V_{CC} = 5.5\text{ V};$ one input at 3.4 V, other inputs at $V_{CC}$ or GND [2]	-	-	2.5	mA
$C_I$	input capacitance	control pin; $V_I = 3\text{ V or } 0\text{ V}$	-	3.2	-	pF
$C_{io(off)}$	off-state input/output capacitance	port off; $V_I = 3\text{ V or } 0\text{ V}; n\overline{OE} = V_{CC}$	-	6.5	-	pF
$R_{ON}$	ON resistance	$V_{CC} = 4.5\text{ V}; V_I = 0\text{ V}; I_I = 64\text{ mA}$ [3]	-	3.6	5	$\Omega$
		$V_{CC} = 4.5\text{ V}; V_I = 0\text{ V}; I_I = 30\text{ mA}$ [3]	-	3.6	5	$\Omega$
		$V_{CC} = 4.5\text{ V}; V_I = 2.4\text{ V}; I_I = 15\text{ mA}$ [3]	-	17	35	$\Omega$

[1] All typical values are at  $V_{CC} = 5\text{ V}, T_{amb} = 25\text{ °C}$ .

[2] This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

[3] Measured by the voltage drop between the nA and the nB terminals at the indicated current through the switch. ON resistance is determined by the lowest voltage of the two (nA or nB) terminals.

10.1. Typical pass voltage graphs

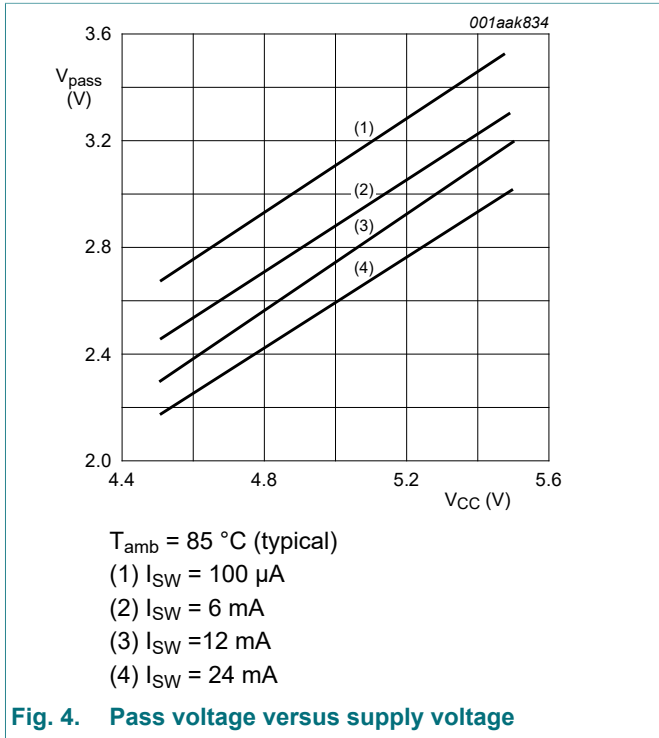


Fig. 4. Pass voltage versus supply voltage

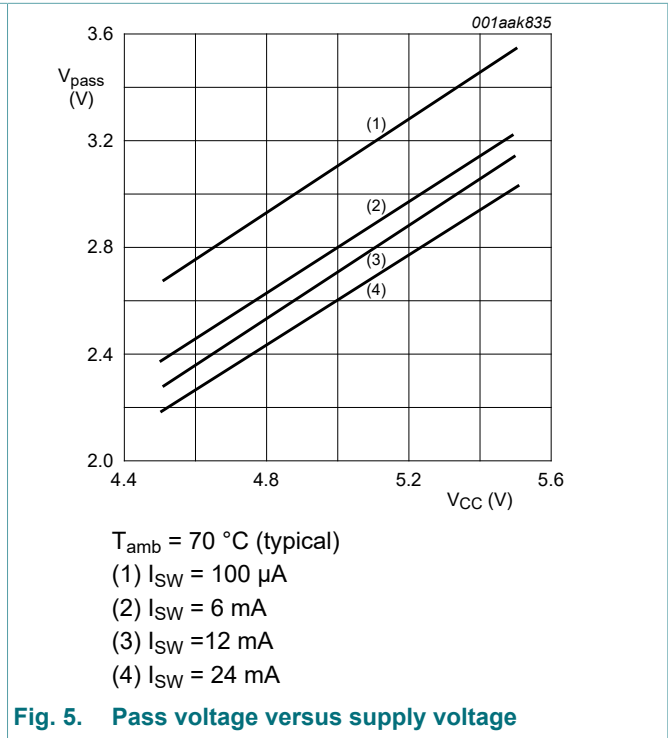


Fig. 5. Pass voltage versus supply voltage

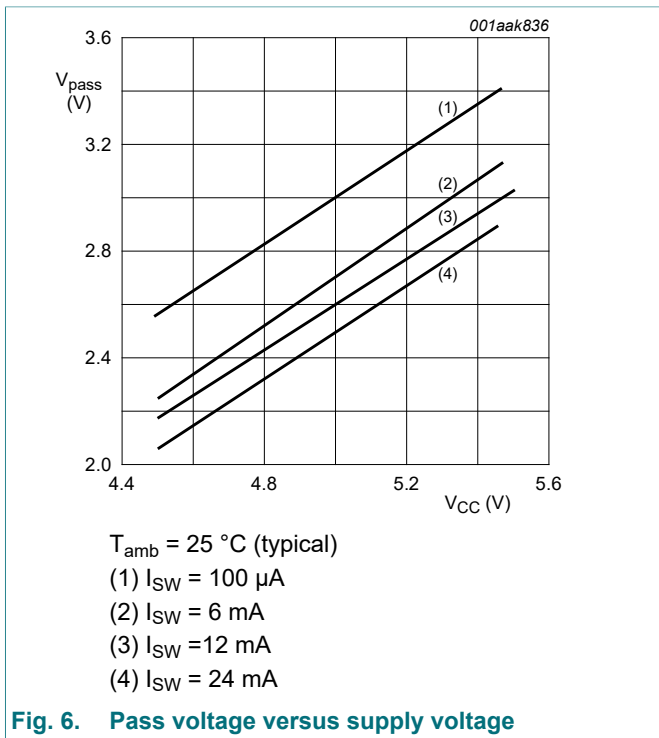


Fig. 6. Pass voltage versus supply voltage

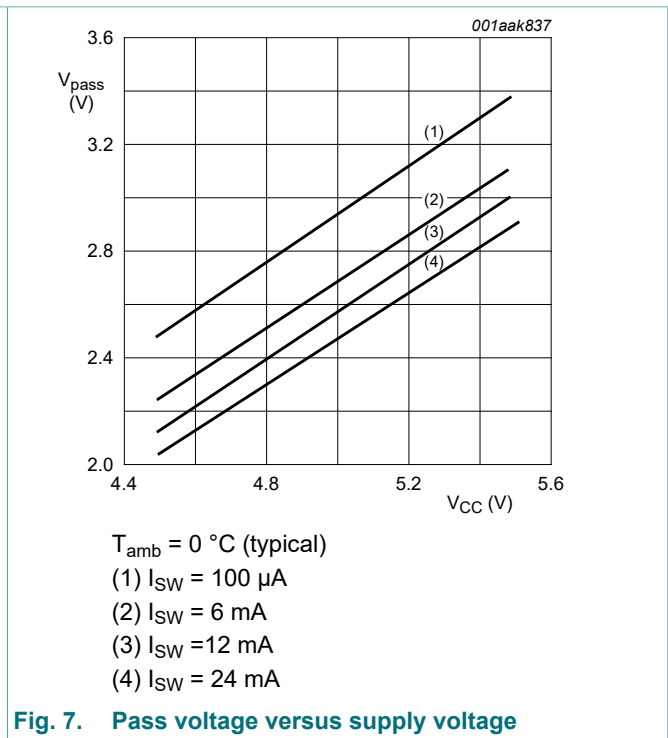
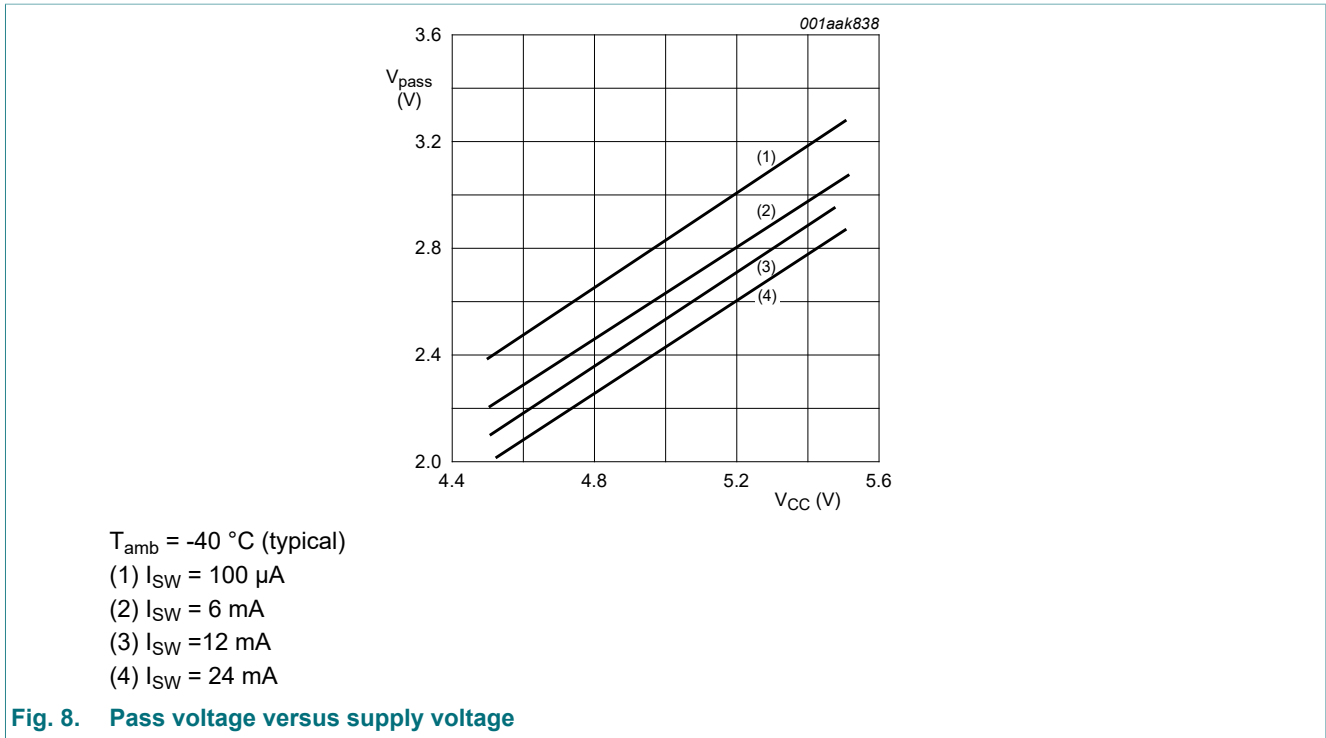


Fig. 7. Pass voltage versus supply voltage



## 11. Dynamic characteristics

**Table 8. Dynamic characteristics**

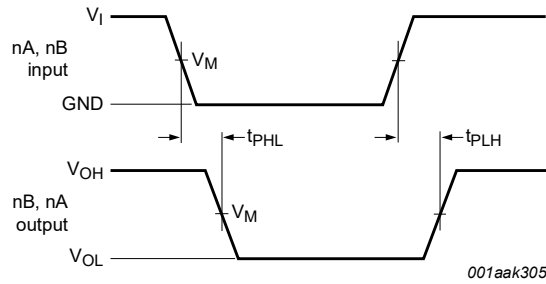
*Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 11.*

Symbol	Parameter	Conditions	$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$			Unit
			Min	Typ	Max	
$t_{pd}$	propagation delay	nA, nB to nB, nA; see Fig. 9 [1] [2]	-	-	0.25	ns
		$V_{CC} = 5.0\text{ V} \pm 0.5\text{ V}$				
$t_{en}$	enable time	n $\overline{O}E$ to nA or nB; see Fig. 10 [2]	1.0	-	5.4	ns
		$V_{CC} = 5.0\text{ V} \pm 0.5\text{ V}$				
$t_{dis}$	disable time	n $\overline{O}E$ to nA or nB; see Fig. 10 [2]	1.0	-	4.9	ns
		$V_{CC} = 5.0\text{ V} \pm 0.5\text{ V}$				

[1] The propagation delay is the calculated RC time constant of the typical ON resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

[2]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ ;  $t_{en}$  is the same as  $t_{PZL}$  and  $t_{PZH}$ ;  $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ .

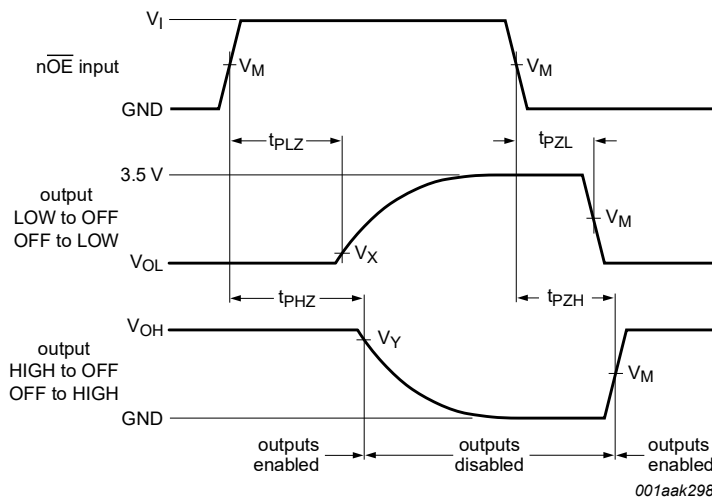
### 11.1. Waveforms and test circuit



Measurement points are given in [Table 9](#).

Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig. 9. The data input (nA, nB) to output (nB, nA) propagation delay times**



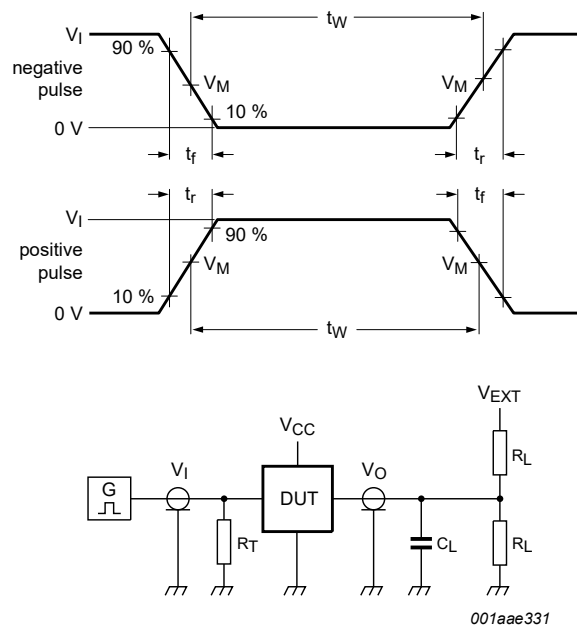
Measurement points are given in [Table 9](#).

Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig. 10. Enable and disable times**

**Table 9. Measurement points**

Supply voltage	Input		Output		
$V_{CC}$	$V_I$	$V_M$	$V_M$	$V_X$	$V_Y$
$V_{CC} = 5.0\text{ V} \pm 0.5\text{ V}$	GND to 3.0 V	1.5 V	1.5 V	$V_{OL} + 0.3\text{ V}$	$V_{OH} - 0.3\text{ V}$



Test data is given in [Table 10](#).

All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z<sub>o</sub> = 50 Ω.

The outputs are measured one at a time with one transition per measurement.

Definitions for test circuit:

R<sub>L</sub> = Load resistance.

C<sub>L</sub> = Load capacitance including jig and probe capacitance.

R<sub>T</sub> = Termination resistance should be equal to output impedance Z<sub>o</sub> of the pulse generator.

V<sub>EXT</sub> = External voltage for measuring switching times.

**Fig. 11. Test circuit for measuring switching times**

**Table 10. Test data**

Supply voltage	Input		Load		V <sub>EXT</sub>		
	V <sub>I</sub>	t <sub>r</sub> , t <sub>f</sub>	C <sub>L</sub>	R <sub>L</sub>	t <sub>PLH</sub> , t <sub>PHL</sub>	t <sub>PLZ</sub> , t <sub>PZL</sub>	t <sub>PHZ</sub> , t <sub>PZH</sub>
V <sub>CC</sub> = 5.0 V ± 0.5 V	GND to 3.0 V	≤ 2.5 ns	50 pF	500 Ω	open	7.0 V	open

## 12. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 4.4 mm

SOT530-1

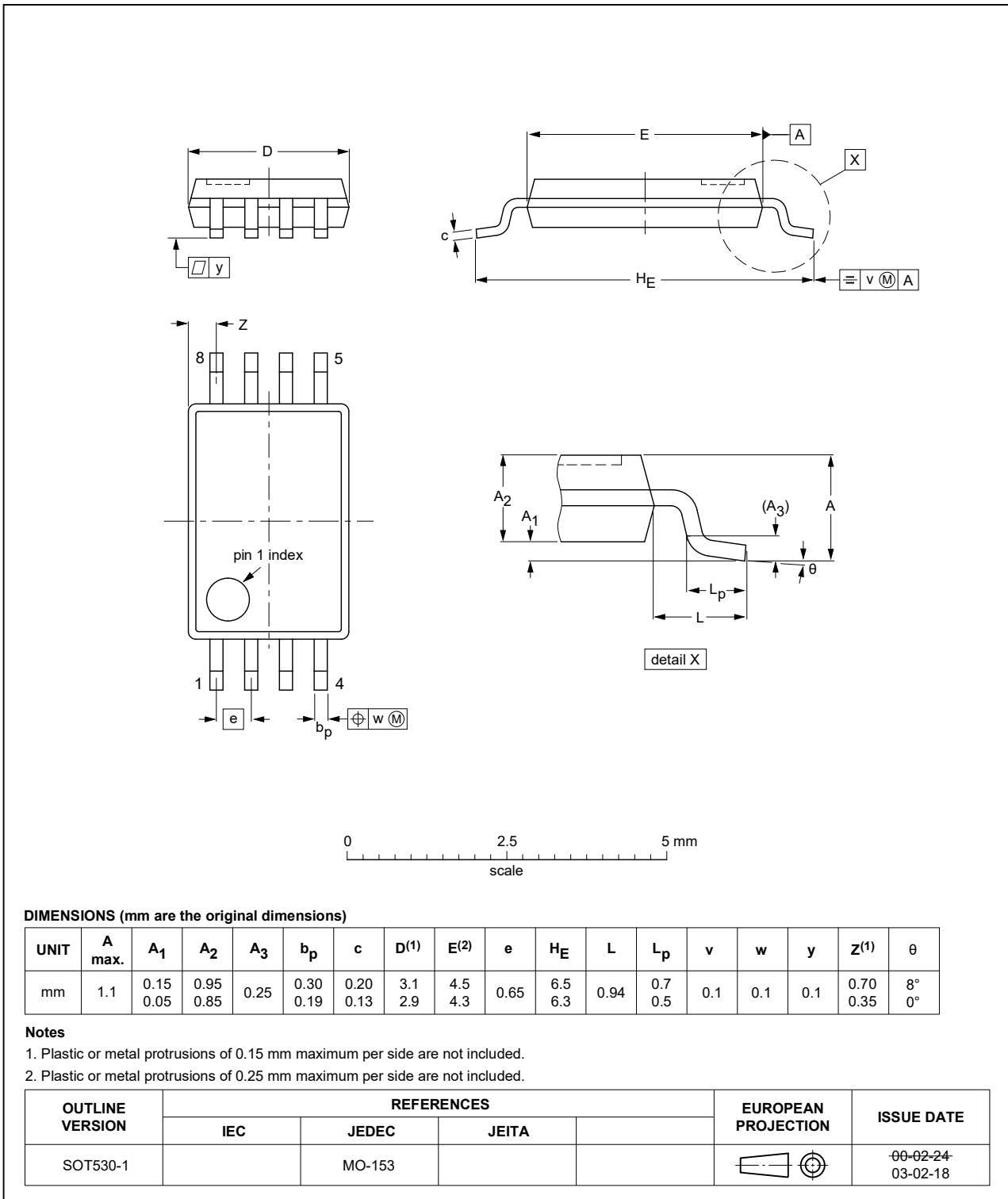


Fig. 12. Package outline sot530-1 (TSSOP8)



XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm

SOT833-1

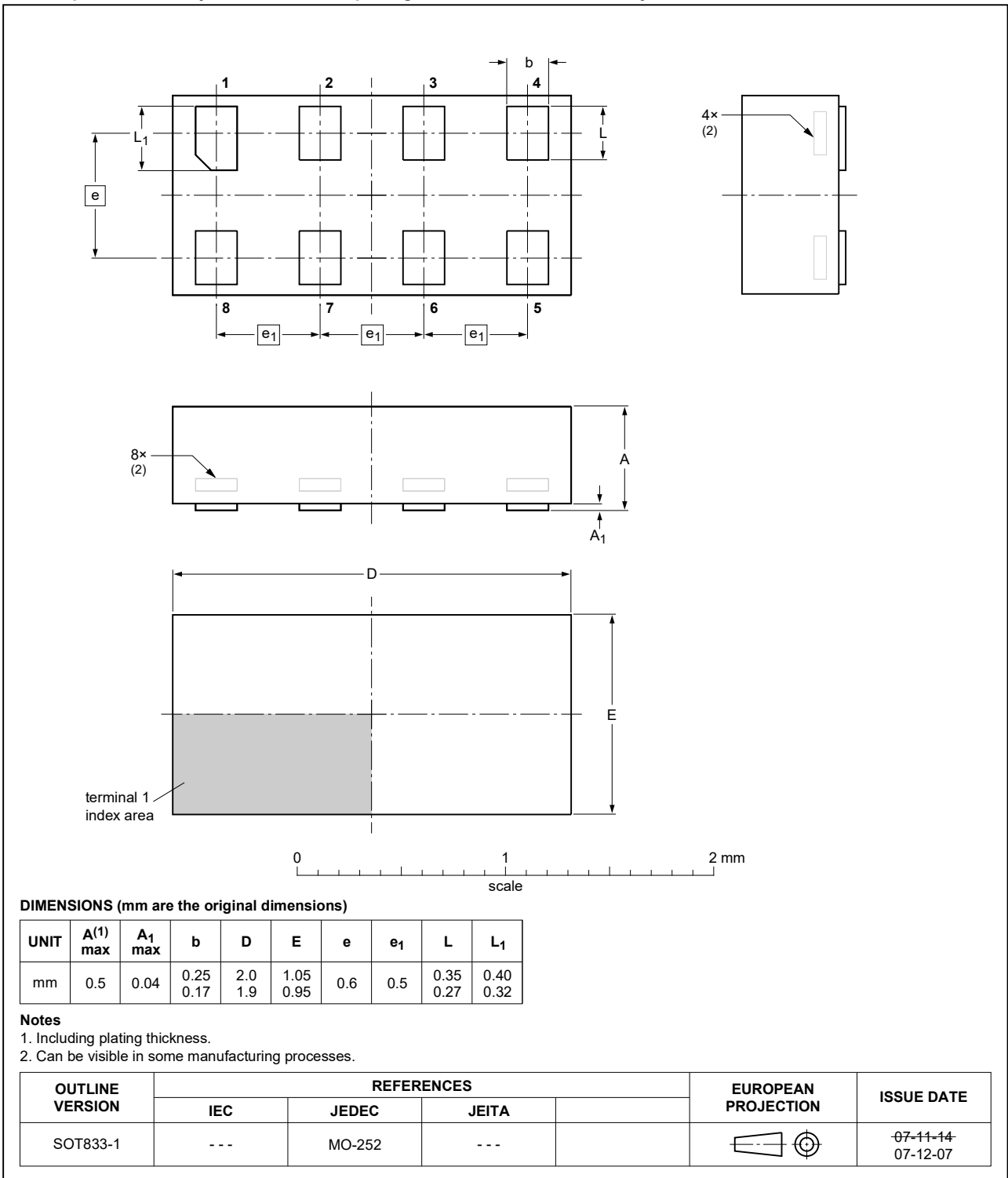


Fig. 13. Package outline SOT833-1 (XSON8)

## 13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
ESD	ElectroStatic Discharge
FET	Field Effect Transistor
HBM	Human Body Model
PRR	Pulse Rate Repetition
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
CBTD3306 v.10	20210319	Product data sheet	-	CBTD3306 v.9
Modifications:	<ul style="list-style-type: none"> <li>Type number CBTD3306GM (SOT902-2 / XQFN8) removed.</li> </ul>			
CBTD3306 v.9	20181115	Product data sheet	-	CBTD3306 v.8
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Type number CBTD3306D (SOT96-1/SO8) removed.</li> </ul>			
CBTD3306 v.8	20120501	Product data sheet	-	CBTD3306 v.7
Modifications:	<ul style="list-style-type: none"> <li>For type number CBTD3306GM the SOT code has changed to SOT902-2.</li> </ul>			
CBTD3306 v.7	20120103	Product data sheet	-	CBTD3306 v.6
Modifications:	<ul style="list-style-type: none"> <li>Marking code for type number CBTD3306D changed.</li> </ul>			
CBTD3306 v.6	20111121	Product data sheet	-	CBTD3306 v.5
Modifications:	<ul style="list-style-type: none"> <li>Legal pages updated.</li> </ul>			
CBTD3306 v.5	20110428	Product data sheet	-	CBTD3306 v.4
CBTD3306 v.4	20100325	Product data sheet	-	CBTD3306 v.3
CBTD3306 v.3	20100223	Product data sheet	-	CBTD3306 v.2
CBTD3306 v.2	20091015	Product data sheet	-	CBTD3306 v.1
CBTD3306 v.1	20011108	Product data	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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- [2] The term 'short data sheet' is explained in section "Definitions".
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